REMARKS

The final Official Action dated October 22, 2003 has been received and its contents carefully noted. In view thereof, claims 38, 41-43, 46-51 and 57-59 have been amended to correct informalities noted by the Examiner and to recite that the lower electrode is a "metal", and further, new claim 60 has been added in order to better define the annealing process temperature, which is supported by the specification at pages 12-13. Accordingly, claims 38-60 are remain pending in the instant application.

The Applicants would like to thank the Examiner for the courtesies extended to the Applicants' representatives during the personal interview of January 14, 2004.

Initially, the Applicants have noted the amendment to the title which has been carried out by the Examiner and agree with the new language for the title.

Turning to the finality of the October 22, 2003 Office Action, the Examiner has stated therein that the "Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action." However, a review of the earlier Amendment of July 21, 2003 (adding new claims 38-59) and the previous Amendment of February 11, 2003 (containing claims 11-37) is that new claim 38 contained the additional step "(d) forming an upper electrode on the capacitive insulating film" whereas earlier claim 11 did not contain such a step. Additionally, the Applicants note that the Examiner states in the Office Action of February 28, 2003 (and again in the final Office Action) that Satoru et al. teach "a upper capacitor electrode 10 formed on the dielectric layer." Therefore, the amendments to at least claim 38 does not appear to have been necessitated by amendment as is required for an office action to be made final, pursuant to MPEP Chapter 706.07(a). Further, a review of REMARKS section of each of the above Amendments reveals that the Applicants have consistently argued that the Sun et al article did not teach annealing the lower electrode before forming the dielectric film, and it is clearly evident from a reading of the instant final Office Action that the newly cited Watanabe et al. ('379) is asserted to teach such a feature that was lacking in the Sun et al article. Therefore, the new ground of rejection was NOT necessitated by the earlier Amendment of July 21, 2003, but instead was necessitated by the Examiner's decision to acquiesce to the

Applicants' arguments regarding the Sun et al article and replace that teaching with the teachings of Watanable et al. Setting forth a new ground of rejection for this reason does not meet the requirements of MPEP Chapter 706.07(a) for making an office action final. Finally, it is noted the that Office Action is not approved/signed by a Primary Examiner, see MPEP Chapter 707.09 For such reasons, it is respectfully requested that the finality of the Office Action of October 22, 2003 be withdrawn and further that this amendment be entered as a matter of right pursuant to 37 C.F.R. 1.111(a).

With regard to the rejection of claims 38, 40, 43-50 and 52-59, under 35 U.S.C. §103(a), as being unpatentable over Satoru et al. (JP '770) in view of Watanabe et al. ('379), this rejection is respectfully traversed. Specifically, the newly presented claim 38 sets forth the following features:

> A method for fabricating a semiconductor device, the method comprising the steps of:
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> a) forming a metal lower electrode on a substrate;
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> b) annealing the metal lower electrode in a reducing atmosphere that contains impurity atoms;
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> c) forming a capacitive insulating film on the metal lower electrode after the step b); and
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> d) forming an upper electrode on the capacitive insulating film,
>
> wherein the impurity atoms are introduced into the metal lower electrode in the step b). (Emphasis Added)

A review of the Satoru et al. patent document reveals that the invention discussed therein is for the purpose of reducing the leakage current by reducing the roughness of the lower electrode of a memory element. This is achieved by annealing the lower (Pt) electrode at elevated temperature (e.g. > 500°C) to make the surface of the lower (Pt) electrode smooth. Satoru et al. document does not teach, as the Examiner has admitted several times previously, annealing in reducing atmosphere such that impurity atoms are introduced into the lower electrode before forming a capacitive insulating film as presently claimed. To remedy that deficiency, the Examiner now relies upon the Watanable et al. patent.

However, a detailed review of the Watanabe et al. patent reveals that the patentees desire to improve memory cells composed of stacked capacitors (column 1,

lines 17-47, 55-67; column 2, lines 1-4) by increasing the effective area of the silicon electrodes, and, further, that as the smaller DRAMs are developed it is becoming difficult to form the insulating films uniformly (without defects) on the silicon surface. To achieve the desired results, the patentees note that it has been known to increase the effective area of silicon electrodes by coating the silicon with SOG (glass) and then micro-roughening by etching. This process has encountered several difficulties; therefore, Watanabe et al. teach replacing the micro-roughening by etching with a new process which employs a micro-roughening by grain growth (column 2, lines 4-25) using two methods. The second method of micro-roughening taught by the patentees (column 5, lines 4-39; column 12, lines 29-38) envisions overcoming the lack of compactness (density) of the first method of micro-roughening by performing, prior to the deposition of the insulation layer, an annealing heat treatment in an argon (inert) atmosphere. It is further stated that such a heat treatment can take place during the impurity doping step (to form the various conductive regions in the silicon of the capacitor, as stated in Embodiments 1-4 where phosphorus is used as the dopant). This process yields a micro-roughened silicon electrode having the ability to receive thinner and more uniform insulating layers thereon. It is of particular importance to note that Watanabe et al. state that the annealing in argon (column 12, lines 28-54) results in the beneficial micro-roughening, and that the addition of dopants, such as phosphorus, arsenic or boron, to the silicon can create micro-roughness in the silicon surface (column 11, lines 48-55). Finally, it is further noted that the patentees teach that the introduction of hydrogen into to the silicon, for the purpose of controlling the generation density of the nucleation sites of the silicon (column 6, lines 5-10; column 11, lines 30-47), occurs not during the annealing heat treatment, but instead occurs during the deposition/growth of the silicon layer.

As can be seen from the above summary, Satoru et al perform an annealing heat treatment to smooth the surface of the (platinum) electrode of a memory in order to reduce the leakage current; while, Watanabe et al. teach performing an annealing heat treatment, without or without a dopant impurity, to micro-roughen the surface of a silicon electrode in the stacked capacitors of a memory in order to achieve a more uniform deposition of the capacitive insulating layers thereon. Clearly, one of

ordinary skill in the prior art would NOT be motivated to modify the teachings of Satoru et al. to instead micro-roughen the platinum electrode since such would be contrary to the intended purpose of Satoru et al. to form a more smooth surface on the electrode to reduce the leakage current, see MPEP Chapter 2143.01 @ page 2100-127.

Accordingly, it is respectfully submitted that neither Satoru et al. or Watanabe et al. suggest that the impurity atoms are introduced into the lower metal electrode before forming the capacitative insulating film via a reducing annealing treatment employing impurity atoms such that the impurity atoms are in a sufficient amount to avoid coagulation and the formation of voids in the metal lower electrode when subjected to elevated temperatures. Consequently, the rejection, under §103(a) , of claims 38, 40, 43-50 and 52-59 has been set forth in error and must now be withdrawn.

With regard to the teachings of:

Andricacos et al. ('609) – cited to teach stacked electrodes of capacitor can be made of Rhodium,

Ichiro et al. (JP '945) – cited to teach that hydrogen atoms, induced into platinum electrodes by heat treatment in an atmosphere containing hydrogen, are detrimental to PZT layers in contact therewith and can be alleviated by heat treatment with an oxygen atmosphere, and the

Saide et al. ('938) reference – cited to teach the formation of a recess in an insulating film prior to carrying out steps a)-d),

a review of each reference reveals that none of these secondary references cures the deficiency of Satoru et al. or Watanabe et al. To the contrary, the Ichiro et al patent document states that the presence of hydrogen in the platinum electrode is undesirable for its effects on the PZT insulating layers and can be prevented by heat treatment in an atmosphere containing oxygen.

Accordingly, the rejections of claims 39, 41, 42 and 51, under §103(a), based upon the teachings of Satoru et al. and Watanabe et al., along with the above identified secondary references, do not disclose or remotely suggest the presently claimed features. Consequently, the rejections, under §103(a), of claims 39, 41, 42 and 51 have been set forth in error and must now be withdrawn.

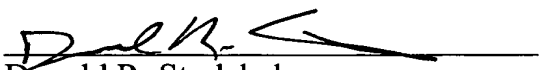
With respect to new claim 60, Applicants respectfully submit that the combination proposed by the Examiner fails to disclose or suggest that the annealing

process is performed at the temperature of 450 - 500°C, which finds support at page 12, lines 24. Accordingly, it is respectfully submitted that new claim 60 is likewise in condition for allowance.

In summary, in view of the foregoing amendments and reasons, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that newly amended claims 38-60 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,



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